

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are presently active, and Claims 1, 7, and 13 are amended by the present amendment. Support for the amendment is found on page 14, lines 9-16, and Figures 6 and 7. Thus, no new matter is added.

In the outstanding Official Action, Claims 1-20 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,683,767 to Ito et al. (hereinafter “Ito”) in view of U.S. Patent No. 5,637,900 to Ker et al. (hereinafter “Ker”) and U.S. Patent No. 5,745,323 to English et al. (hereinafter “English”).

Applicants acknowledge with appreciation the telephonic interview granted on September 7, 2006, between Applicant’s representative and the Examiner, where the Examiner acknowledged that the outstanding Official Action did not include a period for reply.

Claim 1 is directed to a semiconductor integrated circuit device comprising an inner circuit driven by a single power voltage, and a first protective circuit which protects the inner circuit from a surge. The inner circuit includes a high voltage-proof circuit section constituted of a first MOS transistor; a low voltage-proof circuit section constituted of a second MOS transistor including a gate insulating film thinner than that of the first MOS transistor; and a second protective circuit directly connected to the low voltage-proof circuit section to protect the second MOS transistor from the surge. Claim 1 is amended to recite that “data is transferred from the first protective circuit to the second protective circuit.”

The outstanding Official Action acknowledges that Ito and Ker fail to disclose or suggest a first protective circuit, but finds that English discloses this feature.¹

¹ See Official Action, August 24, 2006 at pages 2 and 3.

English describes a tri-state inverter (110) having a circuit (230) for ESD protection.² The circuit (230) comprises an NMOS transistor (232) with the gate (234) and drain (238) of the transistor are connected to the power supply VDD, and the source (236) connected to ground.³ However, English fails to disclose or suggest that data is transferred from a first protective circuit to a second protective circuit.

Claim 1 is distinguishable over English as the applied reference fails to disclose “that data is transferred from a first protective circuit to a second protective circuit.” As the circuit (230) is configured to provide ESD protection for an inverter, the protective circuit (230) cannot receive data since the gate (234) and drain (238) of the transistor are connected to the power supply VDD, while the source (236) is connected to ground. Since the protective circuit (230) of English cannot receive data, logic dictates that data cannot be transferred from circuit (230) to a second protective circuit.

Therefore, it is respectfully submitted that combining the circuit (230) of English with the circuits described in Ker and Ito would fail to disclose or suggest a first protective circuit and a second protective circuit where “data is transferred from the first protective circuit to the second protective circuit.” Accordingly, it is respectfully submitted that the rejections of Claim 1, and claims dependent therefrom, under 35 U.S.C. § 103(a) are overcome by the present amendment to Claim 1.

Similar arguments apply to amended Claims 7 and 13. Accordingly, it is respectfully submitted that the rejections of Claims 7 and 13, and claims depending therefrom, under 35 U.S.C. § 103(a) have also been overcome by the present amendment to Claims 7 and 13.

² See English at column 5, line 65 to column 6, line 2 and Figure 6.

³ See English at column 6, lines 3-12.

Consequently, in view of the present response, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. A Notice of Allowance for Claims 1-20 is earnestly solicited.

Respectfully submitted,

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